EE 417 Responsibility Breakdown DOR

0. Solution code typed in and checked Kalin

1. The design should implement the Datapath-controller structure. Jammeh

2. There should be real application for your design. Examples that you may consider are:

- DSP algorithms:

Integrator with serial input

Differentiator with serial input

Linear Interpolator to increase the data rate.

**Moving Average <<selected>>**

FIR filter using MAC

IIR filter using MAC

Non-Linear Energy Operator: y[n] = x2[n] – x[n-1]x[n+1]

- FIFO design with read and write address pointers.

- Parallel-to-Serial converters between two different clock domains

- Applying/Designing data transmission protocols with packet formations

3. The use of pipelining would be given extra credit. Jammeh

4. The design should include a testbench to verify the results. The testbench input data and results can

be saved as a text file and plotted in MATLAB (or Excel) for extra credit. Kalin

5. Timing Analysis should be included. Jammeh

6. The Verilog Code should be well documented and explained. Kalin

The final presentation should include:

1. A brief description of the objective and application of the design. Kalin

2. A block diagram that clearly shows the Datapath-controller structure of your design with the datapath

and control signals distinctly presented. Kalin

3. The state graph of the controller Kalin

4. The building blocks of the datapath. Jammeh

5. The Verilog code. Jammeh

6. Simulation results in Questa showing specific cases, such as reset, dataflow between registers with

expected delays … etc. Use internal probes as needed to verify the functionality. Jammeh/Kalin

7. Timing analysis report information.showing the maximum throughput or clock frequency that can be

implemented on your design. Jammeh/Kalin